REMARKS

Claims 10-36 are pending in the Application and all were rejected in the Office action mailed April 10, 2008. No claims are amended by this response. Claims 10 and 24 are independent claims, while claims 11-23 and 25-36 depend either directly or indirectly from independent claims 10 and 24, respectively. Applicants respectfully request reconsideration of claims 10-36, in light of the following remarks.

The Applicants note that a goal of patent examination is to provide a prompt and complete examination of a patent application.

> It is essential that patent applicants obtain a prompt yet complete examination of their applications. Under the principles of compact prosecution, each claim should be reviewed for compliance with every statutory requirement for patentability in the initial review of the application, even if one or more claims are found to be deficient with respect to some statutory requirement. Thus, USPTO personnel should state all reasons and bases for rejecting claims in the first Office action. Deficiencies should be explained clearly, particularly when they serve as a basis for a rejection. Whenever practicable, USPTO personnel should indicate how rejections may be overcome and how problems may be resolved. A failure to follow this approach can lead to unnecessary delays in the prosecution of the application.

M.P.E.P. §2106(II) (emphasis added).

As such, the Applicants assume, based on the goals of patent examination noted above, that the current Office Action sets forth "all reasons and bases" for rejecting the claims.

Applicants respectfully note that no claims are amended by this response. However, Applicants respectfully submit that the Office has misinterpreted the teachings of the references, and respectfully request that the cited references and the following remarks be thoroughly considered by the Office, to avoid the need to proceed to appeal.

Rejection of Claims

Claims 10-36 were provisionally rejected on the ground of non-statutory obviousness-type double patenting over claims 34-58 of co-pending Application No. 10/170,019. Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872, hereinafter "Krishnamurthy"). Claims 13 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Bruck (US 6,519,289). Claims 14, 17-19, 27, 30-32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Hinchley et al. (US 6,490,250, hereinafter "Hinchley"). Claims 21-23 and 34-36 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Boice et al. (US 6,823,013, hereinafter "Boice"). Applicants respectfully traverse the rejections.

With respect to the rejections under 35 U.S.C. §103(a), Applicants respectfully submit that the Office action has failed to establish a *prima facie* case of obviousness, in accordance with M.P.E.P. §2142. According to M.P.E.P. §2142, "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." M.P.E.P. §2142 further states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." As recognized in M.P.E.P. §2142, "[t]he Supreme Court in *KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007), 82 USPQ2d 1385, 1396 noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit." In addition, the Federal Circuit has made clear that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). See also *KSR,* 127 S. Ct. 1727 (2007), 82 USPQ2d at 1396.

I. Non-Statutory Double Patenting

Claims 10-36 were rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 34-58 of U.S. Patent Application Serial No. 10/170,019. Applicants do not agree with the Examiner's rejection, but nevertheless are submitting a Terminal Disclaimer in compliance with 37 C.F.R. 1.321(c), disclaiming the terminal part of this application that extends beyond the expiration date of commonly owned U.S. Patent Application Serial No. 10/170,019, to obviate the double patenting rejection. Applicants respectfully submit that the obviousness-type double patenting rejection is overcome.

II. Krishnamurthy Does Not Render Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 Unpatentable

Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872, hereinafter "Krishnamurthy"). Applicants respectfully note that the Office relies only upon Krishnamurthy in the rejection of claims 10-12, 15-16, 20, 24-25, 28-29, and 33.

According to Krishnamurthy at column 1, lines 15-19, Krishnamurthy "…relates to the compression and transmission of video signals, and, in particular, to the compression and transmission of multiple compressed video streams over a **single**, shared communication channel." (emphasis added)

With regard to independent claim 10, Applicants respectfully submit that claim 10 recites, in part, "…[a] single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio; … wherein the device transmits

the first multiplexed stream to circuitry external to the device via a first output of the device; and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device." Applicants respectfully submit that Krishnamurthy does not teach this aspect of Applicants' claim 10.

Applicants first address the teachings of Fig. 3 of Krishnamurthy, many of the elements of which are cited by the Office. Fig. 3 of Krishnamurthy is reproduced below:

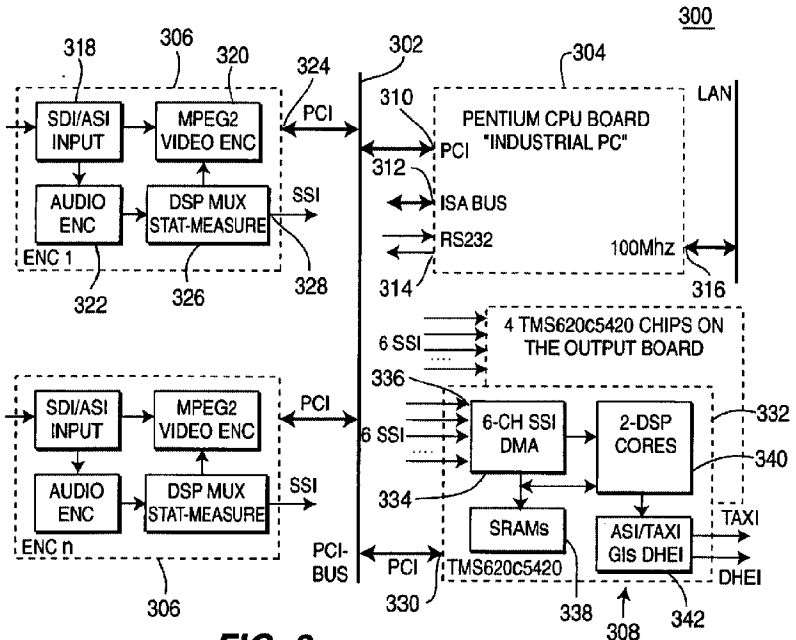

FIG. 3

Krishnamurthy teaches that Fig. 3 is "...a system-level block diagram of computer system, according to one embodiment of the present invention." *See id.* at column 4, lines 8-10. Krishnamurthy describes Fig. 3 in greater detail at column 18, lines 9-19, which is reproduced below:

> FIG. 3 shows a system-level block diagram of computer system 300, according to one embodiment of the present invention. Computer system 300 is a PCI bus-based industrial PC (Personal Computer) enclosure with multiple PCI boards. In particular, computer system 300 comprises a

> PCI bus 302 configured with a Central Processing Unit (CPU) board 304, up to n=24 encoder boards 306, and a statistical multiplexing (stat-mux) board 308. Although computer system 300 relies on a PCI bus, it will be understood that any other suitable system bus could be used in alternative embodiments of the present invention.

It is clear from Fig. 3 and the section of Krishnamurthy arguably the most relevant text portion of Krishnamurthy, that a "computer system" in accordance with an embodiment of Krishnamurthy has a "central processing unit (CPU) board", a number of "encoder boards", and a "statistical multiplexing (stat-mux) board", and that it processes "multiple compressed video streams" for transmission "over a **single**, shared communication channel."

Applicants respectfully submit that Krishnamurthy does not teach or suggest, at least, "…[a] single-chip audio/video encoder device comprising, on a single integrated circuit: … multiplexer circuitry that operates in a first mode and a second mode … wherein the device transmits a first multiplexed stream to circuitry external to the device via a first output of the device; and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device."

The Office asserts that "…Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) comprising … multiplexer circuitry that operates in a first mode and a second mode (col. 20, lines 22-25, "multi-channel mode" would obviously suggest a first mode and a second mode),…." See Office action of April 10, 2008 at page 3. Applicants respectfully disagree. Applicants now address the teachings of Krishnamurthy at column 20, lines 12-25, which is reproduced below, with the cited portion underlined:

> Each SSI serial input port 336 has three wires carrying a clock signal (sclk), a data signal (sdat), and a frame signal. All 24 clock signals sclk should be configured as the input clock signals and connected to an on-board 27-MHz clock oscillator 504. 27-MHz clock 504 will also be used as the DSP clock, and on-chip PLL circuits will generate a

> 90-MHz DSP clock. In that case, on-chip timers can be used for the PCR time-base corrections. The frame signals will indicate whether or not the data signal sdat carries meaningful data. The data signals sdat are burst with a maximum rate of 27 Mbps. The frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters.

The portion of Krishnamurthy shown above teaches that each "SSI serial input port 336" has "clock", "data", and "frame" signals as inputs, and that the "frame" signals will indicate whether the "data" signals carry meaningful data. Krishnamurthy also states that "…The frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters." The cited portion of Krishnamurthy, however, does not teach or suggest a "first mode" and "second mode" of a multiplexer, "…which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; **and** which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio;…", in accordance with Applicants' claim 10.

Applicants respectfully submit that the "multi-channel mode" of Krishnamurthy is related to a "frame signal" used to "send multiple packets into assigned on-chip buffers for transmitting the individual encoders' statistical parameters…", and fails to teach or suggest anything in regard to a "first mode" and "second mode" that relate to how "first compressed audio", "first compressed video", "second compressed audio" and "second compressed video" are multiplexed to form one or two multiplexed streams [wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device], in accordance with

Applicants' claim 10. Therefore, Applicants' respectfully submit that Krishnamurthy at column 20, lines 22-25 fails to teach at least this aspect of Applicants' claim 10.

The Office continues by asserting that Krishnamurthy teaches "…[a] single-chip audio/video encoder device …which when operating in the first mode (308 of fig. 3, the multiplexer (308) for multiplexing up to 24 different channels of transport bitstreams from the MPEG-2 encoders; col. 20, lines 10-11) produces a first multiplexed stream (fig. 5, multiplexing bitstreams and outputting a first multiplexed bitstream) from first compressed video (320 of fig. 3), first compressed audio (322 of fig. 3), second compressed video (ENCn, 320 of fig. 3), and second compressed audio (ENCn, 322 of fig. 3);…." *See* Office action of April 10, 2008 at page 3. Applicants first address Krishnamurthy at column 20, lines 1-11, which has been reproduced below in context, with the cited portion underlined:

> FIG. 5 shows a board-level block diagram of statistical multiplexing board 308 of computer system 300 of FIG. 3, according to one embodiment of the present invention. Stat-mux board 308 is a low-delay Input/Output (I/O) interface PCI board with the statistical multiplexing system and PCR time-base correction firmware. Stat-mux board 308 comprises an internal sub-system bus 502 configured with four Texas Instruments TMS320c5420 DSP chips 332, each having six SSI serial ports 336 and 512 Kbytes of on-chip <u>SRAM memory 338, such that stat-mux board 308 can receive up to 24 different channels of transport bitstreams.</u>

The cited portion of Krishnamurthy shown above simply teaches that an embodiment of a "stat-mux board 308" of Fig. 3 comprises four "TMS320c5420 DSP chips 332" each having six "SSI serial ports 336" and on-chip SRAM, so that "stat-mux board 308" can receive "…up to 24 different channels of transport streams." Applicants now turn to the alleged teachings of Fig. 5 of Krishnamurthy, which has been reproduced below:

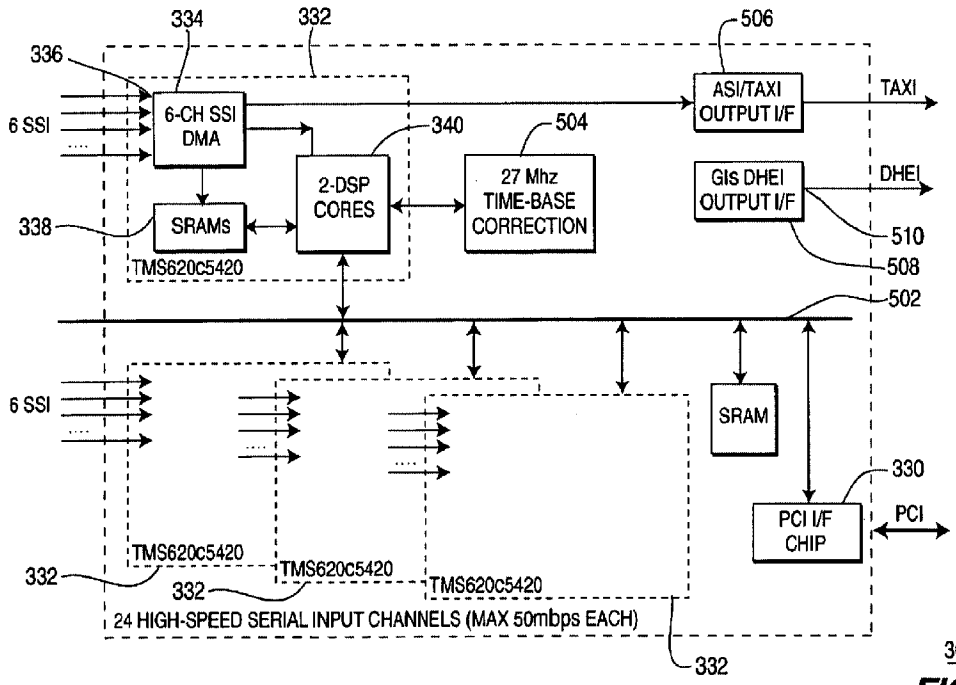

FIG. 5

The cited figure of Krishnamurthy reproduced above illustrates what Krishnamurthy describes as "...a board-level block diagram of the statistical multiplexing board of the computer system of FIG. 3." *See id.* column 4, lines 14-15. The illustration of Fig. 5 shows the "stat-mux board 308" with four "TMS320c5420 DSP chips 332" each having six "SSI serial ports 336", in which one of the "TMS320c5420 DSP chips 332" produces a signal to an element labeled as "ASI/TAXI OUTPUT I/F 506", which produces a signal labeled "TAXI". Krishnamurthy also shows an element "GIs DHEI OUTPUT I/F 508" producing a signal "DHEI 510". Krishnamurthy further describes the "stat-mux board 308" at column 18, lines 42-52, which recites:

> Stat-mux board 308 has a PCI bus interface 330 and four DSP chips 332, where each DSP chip 332 has a six-channel SSI DMA (Direct Memory Address) 334 with six SSI ports 336, SRAMs 338, two DSP cores 340, and an ASI/TAXI.TM. chip set from Advanced Micro Devices, Inc., of Sunnyvale, Calif., and, in block 342, a DHEI (Digital High-speed Expansion Interface) I/O port from General Instrument Corporation (GI) of Horsham, Pa., for GI's modulator and CA

> (Conditional Access) equipment. As such, stat-mux board 308 can support up to 24 channels of low-delay MPEG2 video/audio input bitstreams.

The portion of Krishnamurthy shown above simply repeats some of the teachings at column 20, lines 1-11, and in addition, states that an "ASI/TAXI chip set" and "DHEI I/O port" are provided on the "stat-mux board 308". Based on the above, Applicants respectfully submit that Fig. 5. of Krishnamurthy teaches the multiplexing of signals received on "SSI serial ports 336" to produce one "TAXI" output signal, used to transmit "…multiple compressed video streams over a **single**, shared communication channel…", as stated by Krishnamurthy at column 1, lines 15-19. This portion of Krishnamurthy does not, however, teach or suggest that "stat-mux board 308" of the "computer system" of Fig. 3 produces more than a single multiplexed stream of compressed audio and video for transmission by the "computer system" of Fig. 3, from the "…up to 24 different channels of transport bitstreams from the MPEG-2 encoders…" described in the portions and figures of Krishnamurthy, reproduced above.

The Office asserts that Krishnamurthy teaches "…[a] single-chip audio/video encoder device … which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio (SSI, 328 of fig. 3), and produces a second multiplexed stream (fig. 5, multiplexed bitstreams and outputting a second multiplexed bitstream) from the second compressed video and the second compressed audio (AUDIO ENC and MPEG-2 ENC of fig. 3);…. *See* Office action of April 10, 2008 at pages 3-4. Applicants respectfully disagree.

Applicants have shown above that Fig. 5 of Krishnamurthy does not teach or suggest that the "stat-mux board 308" produces more than one "TAXI" output stream, which Krishnamurthy teaches is used to transmit the multiplexed stream comprising multiple compressed video streams. While Krishnamurthy does disclose that the "encoder board 306" includes a "video encoder 320" ("MPEG-2 ENC" of Fig. 3), an "audio encoder 322" ("AUDIO ENC" of Fig. 3), and a "DSP controller 326" with an "SSI

port 328" (*See id.* at column 18, lines 34-41 and lines 56-60), Krishnamurthy does not teach or suggest that the "video/audio bitstream" transmitted from the "SSI port 328" of the "encoder board 306" is transmitted "…to circuitry external to the device…" via an "…output of the device…", in accordance with Applicants' claim 10. Instead, Krishnamurthy teaches that the output of "SSI port 328" of each "encoder board 306" is "…directly transmitted from the SSI port 328 of the corresponding encoder board 306 to an SSI port 336 on stat-mux board 308." *See id.* at column 18, lines 56-60. Therefore, Applicants respectfully submit that Krishnamurthy does not teach or suggest, at least, Applicants' features "…[a] single-chip audio/video encoder device … which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio … wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device…", as asserted by the Office.

In addition, Applicants respectfully submit that Krishnamurthy does not teach or suggest, at least, Applicants' feature "…[a] single-chip audio/video encoder device … comprising: … control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;…."

The Office action asserts that Krishnamurthy teaches "…[a] single-chip audio/video encoder device … comprising: … control circuitry (304 of fig. 3, note that the CPU (304) is programmable to control all elements, so the CPU would obviously synchronize all elements as described in figure 3) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;…." Applicants respectfully disagree.

Applicants respectfully submit that Fig. 3 of Krishnamurthy fails to teach anything about "synchronizing". Applicants have reproduced Fig. 3 of Krishnamurthy again, below:

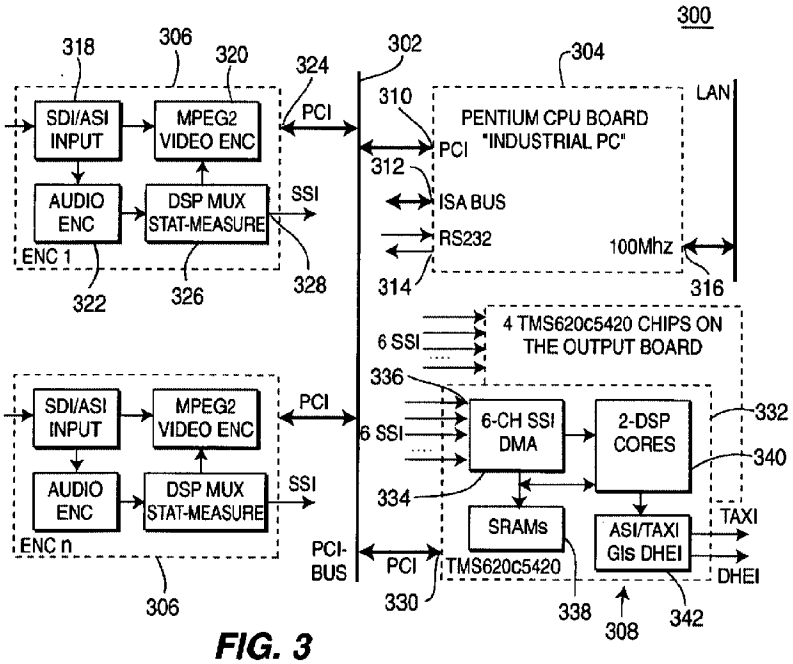

FIG. 3

Applicants respectfully repeat that Fig. 3 of Krishnamurthy simply teaches that Fig. 3 is "...a system-level block diagram of computer system, according to one embodiment of the present invention." *See id.* at column 4, lines 8-10. However, Applicants respectfully submit that nothing in Fig. 3 teaches anything about "synchronization" of "encoders" and "multiplexer circuitry" by "control circuitry", in accordance with Applicants' claim 10.

Krishnamurthy describes Fig. 3 in greater detail at column 18, lines 9-19, which is reproduced again, below:

> FIG. 3 shows a system-level block diagram of computer system 300, according to one embodiment of the present invention. Computer system 300 is a PCI bus-based industrial PC (Personal Computer) enclosure with multiple PCI boards. In particular, computer system 300 comprises a PCI bus 302 configured with a Central Processing Unit (CPU) board 304, up to n=24 encoder boards 306, and a statistical multiplexing (stat-mux) board 308. Although computer system 300 relies on a PCI bus, it will be

> understood that any other suitable system bus could be used in alternative embodiments of the present invention.

Applicants respectfully submit that there is nothing in this portion of Krishnamurthy that says anything about "synchronization" by "CPU board 304", or any other element of Fig. 3. of Krishnamurthy, of the other elements of the "computer system" of Fig. 3, which the Office has identified as teaching Applicants' "single-chip audio/video encoder device". Applicants respectfully note that the Office fails to provide any support for its conclusory statement that "…the CPU would obviously synchronize all elements as described in figure 3…." (emphasis added) *See* Office action of April 10, 2008 at page 4. In the absence of any support, Applicants are left to conclude that the Office is impliedly asserting that synchronization of the "encoder board 306" and "stat-mux board 308", which the Office identified as teaching Applicants' features "first encoder", "second encoder", and "multiplexer circuitry", by the "CPU board 304", is inherent.

According to MPEP §2112, Sec. IV, page 2100-54,55, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is **necessarily** present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, **may not be established by probabilities or possibilities**. The mere fact that a certain thing **may** result from a given set of circumstances **is not sufficient**.'" (emphasis added) In addition, M.P.E.P. §2112 recognizes that the courts have made clear that "In relying upon the theory of inherency, the examiner **must** provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic **necessarily** flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)." (emphasis in original).

Applicants respectfully submit that the Office has failed to provide any basis in fact and/or technical reasoning to reasonably support the determination that "…the CPU would obviously synchronize all elements as described in figure 3…" necessarily flows

from the teachings of the applied prior art. Therefore, Applicants respectfully submit that the Office has failed to show that (CPU board 304) would inherently synchronize the "encoder board(s) 306" and "stat-mux board 308" of the "computer system 300" of Krishnamurthy.

Indeed, Krishnamurthy clearly states, at column 10, line 60 to column 11, line 20:

> **Since the applications are not synchronized at the frame level, a frame-level target is computed for the encoder that will start encoding a frame next (at any given time)**, based on the average MQUANT chosen for that encoder. Using a rate-distortion model linking bit consumption, average MQUANT, and motion compensated distortion, and enforcing constraints on MQUANT, the bit count for a frame can be estimated from prior data. An example of the constraint on MQUANT can be that the quality is uniform across the applications, while ensuring that the temporal rate of change of average MQUANT is within a tolerance threshold. The channel bit rate is divided between the applications according to their respective complexities and relative significance. The complexities are updated on the fly, and the relative significance can be obtained from the results of off-line profiling stored in application profiles server 124.
>
> For the less controllable encoders, only the frame-level target (or average MQUANT) might be able to be communicated to the encoder. For the more controllable encoders, the basic unit of operation will be a slice (e.g., a row of macroblocks). **Because the encoders are not synchronized**, this will require a worst-case buffer requirement of 2 slices. A slice-level target is computed for each controllable encoder based on the frame target, the buffer fullness for that encoder (which is indicative of the buffer delay), and the instantaneous bit rate available after deducting the bits (within a latency window) from the less controllable encoders. The slice targets are also constrained by the fact that MQUANTs cannot change too much within a frame.

The statements by Krishnamurthy in the above text are clear.

If the Office did not mean to assert inherency, then Applicants respectfully submit that the Office has failed to provide any basis or support for its conclusory statement of the obviousness of this aspect of Applicants' claim 10. Applicants respectfully point out that M.P.E.P. §2142 recognizes that the Federal Circuit has made clear that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." Applicants respectfully submit that the Office has failed to provide such an "… articulated reasoning with some rational underpinning to support the legal conclusion of obviousness…", required by the courts. Further, M.P.E.P. §2142 states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." (emphasis added) However, no such "…articulation of the reason(s) why the claimed invention would have been obvious…" has been provided by the Office to support the rejection of this aspect of Applicants' claim 10.

Therefore, Applicants respectfully submit that the Office has failed to show how and why Krishnamurthy teaches that the encoders (i.e., "video encoder 320" of Fig. 3) of the "computer system 300" of Krishnamurthy are synchronized and, therefore, that it is not true that Krishnamurthy teaches that the "CPU board 304" of Krishnamurthy teaches "…control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;…", as recited by Applicants' claim 10. Applicants respectfully submit that Krishnamurthy does not teach or suggest at least this aspect of Applicants' claim 10.

With regard to dependent claim 15, Applicants respectfully submit that claim 15 recites, in part, "…wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device,…." The Office asserts that "…Krishnamurthy further teaches wherein the device comprises at least one bus interface (PCI, 302 and 310 of fig. 3) that is configurable to operate to couple the control circuitry (304 of fig. 3) and at least one

controller external (316 of fig. 3, downloading micro-codes for MPEG-2 encoder ship [sic], 306 of fig. 3, col. 19, lines 22-28) to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals (PCI of fig. 3)." *See* Office action of April 10, 2008 at page 5. Applicants respectfully disagree. Applicants respectfully note that the Office cites only Krishnamurthy as teaching the features of Applicants' claim 15.

Applicants respectfully submit that the Office previously identified the "computer system 300" and the "CPU board 304" of Fig. 3 of Krishnamurthy as teaching Applicants' "single-chip audio/video encoder device" and "control circuitry" of Applicants' claim 10. Applicants respectfully submit that the Office now identifies "PCI Bus 302" and "LAN interface 316" as teaching Applicants' "at least one bus interface" and "at least one controller external to the device" of Applicants' claim 10. Applicants respectfully submit that it is clear to one of ordinary skill in the relevant art after only a brief review of Fig 3, that the "PCI Bus 302" does not operate to couple the "CPU board 304" to the "LAN interface 316". Indeed, Krishnamurthy explains, at column 18, lines 20-26, that the "CPU board 304" has "...a (e.g., 100-MHz) Local Area Network (LAN) interface 316...." Further, Applicants respectfully submit that a "LAN interface 316" is different from and does not teach Applicants' feature "at least one controller." Because the "LAN interface 316" is part of the "CPU board 304", and Krishnamurthy does not teach that the "LAN interface 316" is connected to the "PCI Bus 302", Applicants respectfully submit that "PCI Bus 302" does not operate to couple the "CPU board 304" and the "LAN interface 316", in accordance with Applicants' claim 15. Therefore, Applicants respectfully submit that Krishnamurthy does not teach or suggest at least "...wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device,...", as recited by Applicants' claim 15.

Based at least upon the above, Applicants respectfully submit that the Office has failed to establish a *prima facie* case of obviousness, as required by M.P.E.P. §2142,

and that Krishnamurthy does not teach, suggest, or otherwise render Applicants' claim 10 unpatentable. Further, Applicants respectfully submit that the Office has also failed to show how and where Krishnamurthy teaches or suggests Applicants' claim 15.

Therefore, Applicants respectfully submit that claim 10 is allowable over Krishnamurthy, for at least the reasons set forth above. Because claims 11-23 depend from allowable independent claim 10, Applicants respectfully submit that Krishnamurthy does not render any of claims 11-23 unpatentable, and that claims 11-23 are also allowable over Krishnamurthy. Further, Applicants have shown above that claim 15 is independently allowable over Krishnamurthy. Accordingly, Applicants respectfully request that the rejection of claims 10-12, 15-16, and 20 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

With regard to independent claim 24, Applicants respectfully submit that claim 24 recites limitations similar to those of independent claim 10, and was rejected on the same grounds as independent claim 10, citing the same teachings of Krishnamurthy as those used in the rejection of claim 10. Therefore, Applicants respectfully submit that claim 24 is allowable over Krishnamurthy for at least the reasons set forth above in Applicants' response to the rejection of claim 10. Because claims 25-36 depend either directly or indirectly from independent claim 24, Applicants respectfully submit that claims 25-36 are also allowable over Krishnamurthy, for at least the same reasons. Further, dependent claim 28, which depends from claim 24, was rejected for the same reasons as Applicants' claim 15, which Applicants have shown above is independently allowable. Accordingly, claim 28 is independently allowable over Krishnamurthy. Applicants respectfully request, therefore, that the rejections of claims 24-25, 28-29, and 33 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

III. The Proposed Combination Of Krishnamurthy And Bruck Does Not Render Claims 13 And 26 Unpatentable

Claims 13 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Bruck. Applicants respectfully submit that claims 13 and 26 depend, respectively, from independent claims 10 and 24. Applicants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that Bruck fails to overcome the deficiencies of Krishnamurthy set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of Krishnamurthy and Bruck, Applicants respectfully submit that claims 13 and 26 that depend therefrom, are also allowable, for at least the same reasons. Accordingly, Applicants respectfully request that the rejections of claims 13 and 26 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

IV. The Proposed Combination Of Krishnamurthy And Hinchley Does Not Render Claims 14, 17-19, 27, And 30-32 Unpatentable

Claims 14, 17-19, 27, 30-32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Hinchley. Applicants respectfully submit that claims 14 and 17-19, and claims 27 and 30-32 depend, respectively, from independent claims 10 and 24. Applicants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that Hinchley fails to overcome the deficiencies of Krishnamurthy set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of Krishnamurthy and Hinchley, Applicants respectfully submit that claims 14, 17-19, 27, and 30-32, that depend therefrom, are also allowable, for at least the same reasons.

Further, with regard to claims 14, 17, 27, and 30, Applicants respectfully submit that claims 14 and 27 recite, in part, "…wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data…", while claims 17 and 30

recite, in part, "…wherein the at least one bus interface is configurable to act as a bus master using direct memory access."

Applicants appreciate recognition by the Office that "…Krishnamurthy does not disclose "…external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data; wherein the at least one bus interface is configurable to act as a bus master using direct memory access as claimed." *See* Office action of April 10, 2008 at page 6.

The Office, however, then relies on Hinchley, and states that "Hinchley teaches a first storage external to the device and a second storage external (108 of fig. 1) to the device(120 of figs. 1 and 2) synchronous dynamic random access memory (116 of fig. 1)." Applicants respectfully disagree that Hinchley teaches the features of Applicants' claims 14, 17, 27, and 30. Applicants are puzzled at the reference to "synchronous dynamic random access memory", since Applicants' claims do not recite this feature.

With respect to claims 14 and 27, Hinchley states, at column 3, lines 27-34: "…Multimedia **data 230** is transmitted to the integrated multimedia encoding system 120 from a **data source 108** within computer system 100 or external to computer system 100. The multimedia encoders 208 receive the **data 230** and compress the **data 230** responsive to the compression format being used in the computer system 100, such as the MPEG2 compression standard…." (emphasis added) Applicants respectfully submit that the data stored in "data source 108" is not "compressed data", as recited by Applicants' claims 14 and 27, but that the data from the "data source 108" is compressed by the "multimedia encoders 208". Further, Applicants respectfully submit that Hinchley does not teach that "data source 108" is used as a "frame buffer". Therefore, Applicants respectfully submit that the "data source 108" of Fig. 1 of Hinchley, specifically cited by the Office, does not teach or suggest, at least, "…wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data…", as recited by Applicants' claims 14 and 27, and that claims 14 and 27 are allowable over the proposed combination of Krishnamurthy and Hinchley.

With respect to claims 17 and 30, Applicants respectfully submit that Hinchley fails to even mention "direct memory access", or "DMA", that element "116" of Fig. 1 is identified by Hinchley as "random access memory 116" or "storage medium 116", and that Hinchley does not teach or suggest that "random access memory/storage medium 116" is a "bus interface" or is "…configurable to act as a "bus master" using "direct memory access"…", as recited by Applicants' claims 17 and 30. Therefore, Applicants respectfully submit that the Office has failed to show how and why the proposed combination of references teaches or suggests Applicants' feature "…wherein the at least one bus interface is configurable to act as a bus master using direct memory access…", as recited by Applicants' claims 17 and 30, and that claims 17 ad 30 are allowable over Krishnamurthy and Hinchley.

Applicants respectfully request that the Examiner explain the significance of the statement, at page 6 of the Office action:

> Therefore, taking the teachings of Krishnamurthy and Hinchley, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages synchronous dynamic random access memory (108 and 116 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy to provide an integrated multimedia encoding system which operates with reduced memory storage requirements when needed.

Applicants respectfully note that an element "318" does not appear in Fig. 2 of either Krishnamurthy or Hinchley. An element "318" does appear in Fig. 3 of Krishnamurthy, and is identified by Krishnamurthy as "ASI input port 318". Applicants respectfully submit that "ASI input port 318" of "encoder board 306" of Krishnamurthy receives ""uncompressed digital video data and multi-channel audio data", and that Krishnamurthy does not teach or suggest that "ASI input port 318" acts as a memory interface to "synchronous dynamic random access memory" or as a "bus master", or employs "direct memory access". Therefore, the significance of this statement by the Office is unclear.

Therefore, for at least the reasons set forth above, Applicants respectfully submit that the proposed combination of Krishnamurthy and Hinchley does not teach or suggest, at least, "…wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data…", as recited by Applicants' claims 14 and 27, and "…wherein the at least one bus interface is configurable to act as a bus master using direct memory access…", as recited by Applicants' claims 17 and 30.

Based at least upon the above, Applicants respectfully submit that the Office has failed to establish a *prima facie* case of obviousness, as required by M.P.E.P. §2142, and that claims 14, 17-19, 27, and 30-32 are allowable over Krishnamurthy and Hinchley. Accordingly, Applicants respectfully request that the rejections of claims 14, 17-19, 27, and 30-32 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

V. The Proposed Combination Of Krishnamurthy And Boice Does Not Render Claims 21-23 And 34-36 Unpatentable

Claims 21-23 and 34-36 were rejected under 35 U.S.C. §103(a) as being unpatentable over Krishnamurthy in view of Boice. Applicants respectfully submit that claims 21-23 and 34-36 depend, respectively, from independent claims 10 and 24. Applicants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that Boice fails to overcome the deficiencies of Krishnamurthy set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of Krishnamurthy and Boice, Applicants respectfully submit that claims 21-23 and 34-36 that depend therefrom are also allowable, for at least the same reasons.

Further, with respect to claims 22, 23, 35, and 36, Applicants respectfully submit that claims 22 and 35 recite, in part, "…wherein the plurality of search processors operate in parallel, each upon a different portion of a macroblock…", while claims 23 and 36 recite, in part, "…wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a

plurality of resolutions." Applicants respectfully submit that the proposed combination of Krishnamurthy does not teach or suggest at least these features of Applicants' claims 22, 23, 35, and 36.

The Office admits that Krishnamurthy does not disclose "...each of motion estimation processors comprises a plurality of search processors that operate in parallel upon a single macroblock, and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search) as claimed." *See* Office action of April 10, 2008 at page 7.

The Office then relies upon Boice, and states that "...Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors sub-dividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3)." Applicants respectfully disagree with what Boice allegedly teaches. The Office does not explain how and why the cited portions of Boice teach what is alleged.

Applicants respectfully submit that Boice makes no mention of "resolution", let alone "half pixel search" and "quarter pixel search", as alleged by the Office. Instead, Boice states the following, at column 4, line 66 to column 5, line 21:

> **The process of searching for a best match involves analyzing each unique 16 x 16 rectangular grid of pixels contained within the bounds of the search window in the reference frame.** By example, an 80 x 80 search window would contain 4225 unique 16 x 16 pixel grids. **Each grid contained in the window is analyzed in raster scan order by starting in the upper leftmost corner of the window, obtaining a search result, and moving <u>one pixel row to the right</u> to obtain a second search result.** The process is repeated in successive rows in the window. At each grid position in the search window a computation or search result is performed which involves summing the absolute difference between the luminance pixel values in the macroblock currently being encoded,

> macroblock 30 in frame 22 in the present example, and the corresponding luminance pixel values of the 16 x 16 pixel grid currently being analyzed. There is a one to one correspondence between the number of unique 16 x 16 grids contained within the search window and the number of search results computed. It is apparent that utilizing an extended window 36 affords a greater number of search results as a consequence of the extended window covering additional pixel grids. The probability of obtaining a more optimal best match motion vector is enhanced as a result.

Applicants have search Boice and have been unable to identify any teaching related to searching at "half pixel" and "quarter pixel" resolutions, as alleged by the Office. If Applicants have inadvertently overlooked such a teaching, Applicants respectfully request that the Office identify such teachings by specific citation to column/paragraph and line, and provide a specific and detailed explanation of how and why the cited teachings allegedly disclose Applicants' claimed features.

In addition, the Office cites elements "36", "38", and "40" of Fig. 3 of Boice as teaching Applicants' claims. Fig. 3 of Boice is reproduced below:

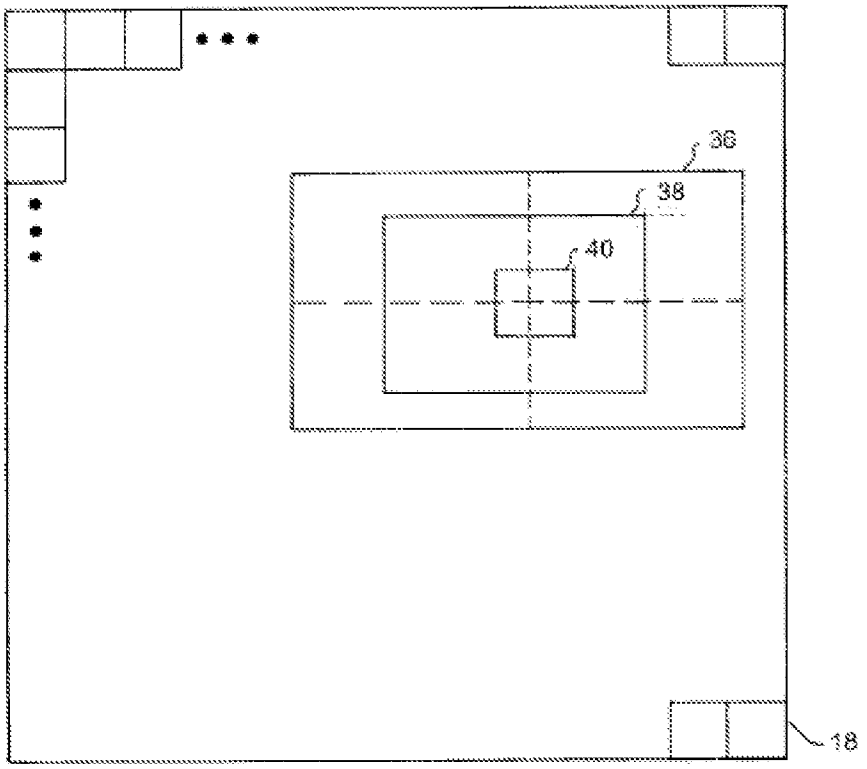

Fig. 3

Applicants respectfully submit that the elements having reference characters "36" and "38" are described by Boice as "extended window 36" and "single encoder configuration window 38". The disclosure of Boice fails to even make reference to an element in Fig. 3 having the reference character "40". While Boice does make reference to element "42", which Boice indentifies as "reference macroblock 42", Boice does not teach or suggest that the "extended window 36", "single encoder configuration window 38", and "reference macroblock 42" represent anything related to "...wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions." Further, the Office has failed to provide a "...some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness...", and instead offers only conclusory statements pointing not to specific portions of the text of Boice, but rather to elements in the figures, without explanation or interpretation.

Therefore, for at least the reasons set forth above, Applicants respectfully submit that the Office has failed to establish a *prima facie* case of obviousness, as required by M.P.E.P. §2142, that the proposed combination of Krishnamurthy and Boice does not teach, suggest, or otherwise render claims 22, 23, 35, and 36 unpatentable, and that claims 22, 23, 35, and 36 are allowable over Krishnamurthy and Boice.

Based at least upon the above, Applicants respectfully submit that claims 21-23 and 34-36 are allowable over Krishnamurthy and Boice. Accordingly, Applicants respectfully request that the rejections of claims 21-23 and 34-36 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Conclusion

In general, the Office has made various statements regarding the claims in the Application and the cited references, which are now moot in light of the above. Thus, Applicants will not address such statements at the present time. However, Applicants expressly reserve the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

The Applicants believe that all of claims 10-36 define allowable subject matter, and request that the Application be passed to issue. Should the Examiner disagree or have any questions regarding this submission, Applicants respectfully invite the Examiner to telephone the undersigned at (312) 775-8000 to resolve any outstanding issues.

A Notice of Allowability is courteously solicited.

The Commissioner is hereby authorized to charge the fee required under 37 C.F.R. §1.17(a)(2) for the Petition, and any additional fees required by this submission, or to credit any overpayments, to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Dated: September 10, 2008

By: /Kevin E. Borg/
Kevin E. Borg
Reg. No. 51,486

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(tel) 312-775-8000
(fax) 312-775-8100